# Helper Cores Using General Purpose Processor Cores As Prefetching Engines In Chip Multiprocessor Architectures

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### Helper Cores Using General Purpose

**Multicore Performance Optimization Using Partner Cores**
Using partner cores and helper threads we are able to achieve application speedup of up to 3x and in-crease power efficiency by up to 22x 2 Architecture At a high-level, a partner core is simply a small, low- This is in contrast with modern general-purpose cores …
**Efficient Emulation of Hardware Prefetchers via Event …**
the idea of using available general-purpose cores in a CMP as helper engines for individual threads running on the ac-tive cores We propose a lightweight architectural frame-work for e cient event …
**Inter-core Prefetching for Multicore Processors Using …**
cores to execute different parts of the serial execution in parallel and then does runtime verification of correctness Mitosis [28] additionally uses helper threads to precompute dependent data Prescient instruction prefetch [1] is another helper …
**Using Asymmetric Cores to Reduce Power Consumption for …**
Using Asymmetric Cores to Reduce Power Consumption such as general-purpose slates or specialized ebook readers Cortex-M3 helper cores (running at up to 384 Mhz) as well as interfaces …

**GePSeA: A General-Purpose Software AccelerationFramework ...**

core architectures and propose GePSeA, a general-purpose software acceleration framework that uses the spare cycles of an available coreinamulti-core equippednode to“onload” complexapplication-specific tasks Specifically, our GePSeA framework provides a lightweight process that acts as a helper ...

**Improving the Performance and Power Efficiency of Shared ...**

ticularly critical in embedded devices designed for general purpose use Here, die area can be efficiently utilized by sharing helper engines among multiple cores [10] In order to resolve these ...

**ProOnE:AGeneral-PurposeProtocolOnloadEngineforMulti-and ...**

The general purpose pro- onload any task using a few of the many available cores Dif-ferent tasks can be added to ProOnE using task-specific plug-tion progress for zero-copy communication using interrupts and helper ...

**Bootstrapping: Using SMT Hardware to Improve Single-Thread ...**

design goal for general-purpose processors Over the years, microarchitectural designs have reached a plateau for the core: while there are more cores, features, and bigger struc-tures today [1], the basic ...

**Bootstrapping: Using SMT Hardware to Improve Single-Thread ...**

(SMT) core as using two cores While fusing two cores can improve single-thread performance by 122x, Bootstrapping provides a speedup of 148 over a broad range of benchmark suites, making it a compelling microarchitectural feature for general-purpose ...

**A Case for Core-Assisted Bottleneck Acceleration in GPUs ...**

tion of the primary threadsSimilar helper threading ideas have been proposed in the context of general-purpose proces-sors [19, 20, 24, 27, 28, 69, 86] to either extend the pipeline with more contexts or ...

**Accelerating Reduction and Scan Using Tensor Core Units**

Tensor Cores — for a total of 640 Tensor Cores and achieve a 12× throughput improvement over previous generation Tesla P100 [54] Google’s TPUv3 device, on the other hand, has 8 cores — 4 chips each with 2 cores ...

**A Framework for Accelerating Bottlenecks in GPU Execution ...**

tion of the primary threadsSimilar helper threading ideas have been proposed in the context of general-purpose proces-sors [22, 23, 27, 31, 32, 97, 122] to either extend the pipeline with more contexts or ...

**Implementation of Embedded Multiprocessor Architecture ...**

design with SoC like integration of less-efficient, general-purpose processor cores with more efficient special-purpose helper engines is project to be the next step in computer evolution [5] First, we aim ...